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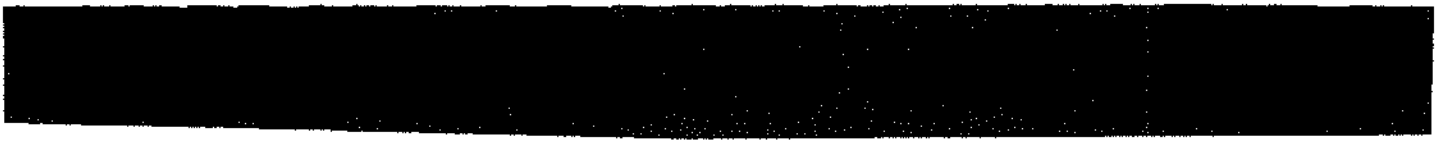
FORCENet Science and Technology
GWOT Focused Tactical Persistent Surveillance

SOW : ONR BAA # 07-014

Multi-modal Agile Sensor Network for GWOT

Subtopic 1: Agile Sensors for GWOT Focused Tactical Persistent Surveillance



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Multi-modal Agile Sensor Network for GWOT Focused Tactical Persistent Surveillance

1 STATEMENT OF WORK

1.1 Technical Concept

The development of multi-modality agile sensors for expeditionary forces must clearly meet the new ISR paradigm for the asymmetric threat. These sensor systems must detect, classify, identify, geo-locate and track low-level threat entities in urban and littoral clutter. To support the GWOT missions, organic sensors for low-level units must be capable of supporting the dynamic character of modern operations from the highly mobile to the long term. These sensors and systems will be mobile and rapidly deployable even in denied areas that are capable of sustained, persistent operation with diverse sensing modalities; inexpensive enough to be procured in very large quantities; small and light enough to cause minimal logistical impact; easy-to-use and networkable.

Avaak proposes to develop a system based on its previous development of wireless sensor systems that provides the following benefits to the warfighter in tactical situations:

- Small, light weight (<1lb) and inexpensive (<$300 in quantities) multifunction sensor that includes imaging, audio, motion and image classification (all in one package).
- Image sensors having sufficient image resolution (2MPixel) and capable of cuing high resolution pan-tilt-zoom cameras.
- On-board image processing and analysis at the node level to minimize data loading through the network and provide actionable data to the warfighter.
- Sensor nodes that can determine their location in relation to other nodes and to global positioning devices (location/situational awareness at the sensor node level).
- Operational capacity of at least 30 days on a replaceable or rechargeable power source.
- Field interoperability with other units/systems.
- Easy deployment, self configuration, automatic alarming and monitoring of certain data parameters. Usable by non-intel units and non-technical personnel.
- Possess a wide area coverage (25Km^2 area or approximately 3Km radius)
- Autonomous, self configuring nodes with capabilities to automatically alarm and monitor for certain data parameters.

1.2 Concept of Operations

The following operational parameters describe the expected duration of the device in the field while operating in two distinct modes.

Mode 1: Continuous Image Transmission from a Multi-Modal Node

[redacted]

While transmitting continuous JPEG video at 4 frames per second it is expected that the multi-modal camera will consume ~40mA of current. Assuming 2 D size lithium 3.7 Volt batteries the battery capacity is expected to be 40AH or 144e6 mA•sec which translates to approximately 41.7 days of operation (or ~6 weeks of continuous video at 4 fps).

Mode 2: Image Processing, Object Characterization and Infrequent Image Transmissions

Image processing and object characterization will be triggered by an event from the (PIR) motion sensor or acoustic sensor. Assuming that the image processor consumes an extra 200mA above the normal system current and the object characterization takes approximately 100msec per image, the total battery capacity required for image processing and object characterization would be 10+200 x.1=30mA•sec. Therefore, operating in continuous image processing/object characterization mode the same battery configuration (2 lithium D cells) shall last for ~14 days (2 weeks processing images at 4 fps).

Thirty days of field operation utilizing this mode would be achieved by utilizing more D cell batteries or a different battery configuration. This mode has the added benefit that it does not consume so much of the network bandwidth (network data loading) thus allowing more nodes to be deployed on the same network and supplying the warfighter with actionable and concrete intelligence when needed.

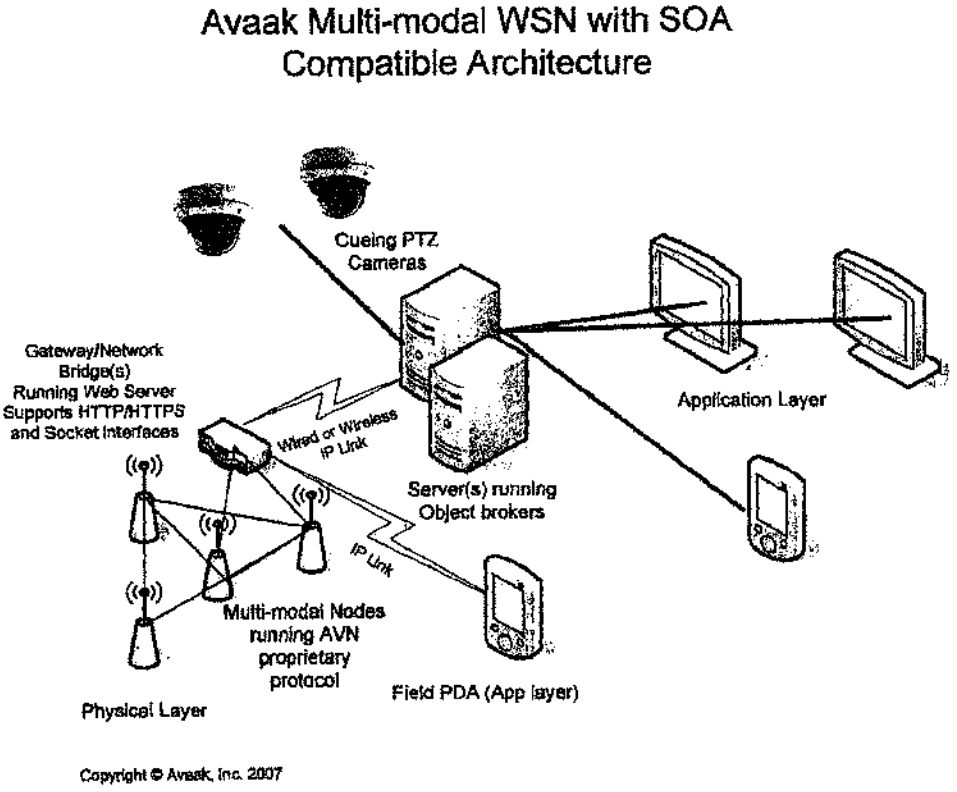

Figure 1 Avaak Multi-modal WSN System Concept

1.3 FY08 Tasks

1.3.1 Task 1 – System Specification for Multi-modal Agile Sensors for GWOT

A detailed specification for a network of multi-mode wireless sensors to provide persistent surveillance will be developed and written as part of this effort. The specification will discuss in detail the different components of the system at the sensor network level (hardware, software and network) as well as image processing algorithms, cross cueing of PTZ cameras, network/gateway functionality and user display application functionality.

The specification will cover the following topics:

- System Specification
  - Requirements Analysis and Review
  - Multi-modal Sensor Node Spec
    - Motion
    - Acoustic
    - Imaging
    - On-board Processing
  - Simple Object Classification Algorithms
    - Low Power Processing Algorithms
    - Tradeoff Analysis
  - High Resolution Camera Queuing
  - Protocol Definition
  - Avaak Vision Network
    - Mesh/Star/Super Star Topology Support
    - TOA and Localization
    - GPS
    - Time Sync Algorithms
    - Localization & Triangulation
  - Radio Range
    - Radio Power Requirements
    - Antenna Characteristics
  - Mechanical Packaging/Size
    - Sensor
    - Base Station
  - Control Software APIs/UI Spec
    - Gateway APIs
    - Simple UI Spec
    - Gateway
    - Capabilities
  - Interfaces

1.3.2 Task 2 – Modifications to the Avaak's Imaging Wireless Network

The Avaak AV18-V Ultra-Miniature Wireless Full Color Camera combines state-of-the-art wireless radio, processing and imaging technology to provide real time imaging in diverse

[redacted]

lighting and environmental conditions. The AV18-V is a self-contained wireless video sensor platform comprised of a digital video imager, a powerful processor, a power source, an antenna system and a miniature radio transceiver circuitry that controls, times, and transmits full color digital video. The AV18-V has extremely low power requirements with battery life maximized through the use of JPEG image compression, patented timing and power saving algorithms and a proprietary wireless protocol. Light sensitivity capability is as low as .5lux-sec. The imaging nodes operate as part of a self-organizing wireless network, with address designation and a custom network protocol that minimizes power consumption for large file transfers. The network is currently configured as a *star* topology in which a centralized hub controls all network activity. For this effort the node will be augmented as follows:

- *Mesh* networking protocol will be implemented to enable sensor to sensor communications
- Localization and time synchronization algorithms will be incorporated into the current firmware.
- The current lens (fixed optics with 60 deg. viewing angle) will be changed to a lens with different optical characteristics (pan/zoom and larger viewing angle)
- Integrate cross-cueing commands and interfaces for networked PTZ cameras
- Add algorithms for simple object recognition on-board
- Extend the RF Range of the node

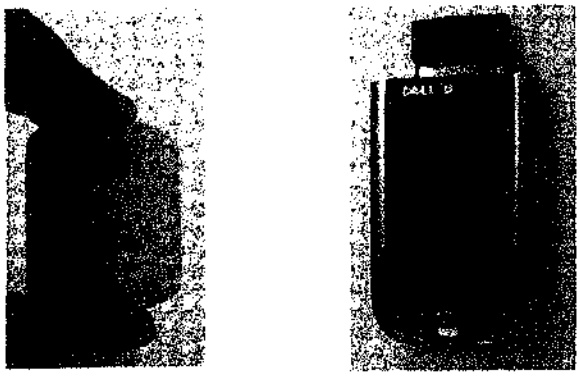

Figure 2 Avaak's AV-18V Ultra-Miniature Wireless Full Color Imager (left). Avaak's portable WSN hub (right) in Compact Flash format

The specifications of the video sensor node will be as follows:

Specifications	**AV-18-V**
Dimensions	~ 1. cubic inch
Weight	< 50grams
Communications range (inbound)	~500 feet for BER<10^{-3}
Communication protocol	Packet switching, frequency hop.

[redacted]

Frequency operating range	2400-2483 MHz ISM band
Modulation type	FSK, GFSK
Frequency step	1MHz
Frequency accuracy	+/-30ppm
Frequency switching speed	<200usec
Data rate (Inbound & outbound)	Programmable:1Mb/s
Imager size	Standard VGA format: 640x480 color pixels, 10 bit A/D
Video Compression	JPEG
Optical viewing angle	60+ degrees
Battery Capacity	>250K transmitted images
Operating temperature	-20 to +70C ambient
RF power output	-10 to +10dBm with 5dB Step
Sensitivity	-100dBm
Antenna	Omni-Directional, >0dBi gain

The Avaak Vision Network™ was demonstrated to the 1st MEF, NECC, SEAL Team 2/Team3 and was included in this year's new technology demonstration at the SeaHawk '07 exercise conducted by NECC in San Diego. Commercial users will also deploy pilot networks for applications in security, asset management and industrial control.

1.3.2.1 Task 2.2 Preliminary Image Processing Algorithm Development

To minimize throughput requirements of the WSN, a certain level of data and signal processing will be performed at the sensor node level so that the communications data rate does not become a bottleneck of the system and so that continuous video feeds from hundreds or thousands of cameras don't over burden the warfighter with unneeded data. By pushing functionality to the edge of the network, sensor nodes are able to make a "certain" level of "decision" based on the sensed data.

Under work currently funded by ONR and DARPA Avaak has commenced development of a small imaging node with on-board image characterization capabilities. Figure 3 shows a picture of a color-changing chemical sensor (porous Si sensor) taken by the Avaak AV-18 miniature camera (left) and subsequent processing performed on the image to characterize color and pattern. Algorithms being developed for this program are specifically geared for low-power, battery-operated miniature camera devices as are being proposed herein.

The thrust of the ongoing development is creating image processing algorithms to detect color and pattern changes specifically tailored for low-power DSP processing on battery operated sensor nodes. An extension of this work, beyond the current focus (chemical sensing), is contemplated for development under this BAA. That effort will consist of determining algorithms and footprints necessary to be located on the sensor nodes (depending on the modalities) in order to balance the power requirement needs of the algorithm with the need to send less data through the network

Figure 3 Image of a Porous Silicon sensor captured by Avaak's Imager node (top left) and process for color variations and pattern extraction (center and bottom right)

1.3.3 Task 3 Addition of Other Sensor Modalities – (Multi-modal Sensor Node)

To alleviate the data throughput and overall power requirements from the imaging nodes, Avaak proposes to supplement its current imaging sensor with motion detection, audio and processing capabilities that will trigger high-resolution cameras or other sensors. These other sensors modalities provide a much more complete view of the tactical environment. The idea is to enable such sensors, which consume less power (for example motion detection by PIR) to create alarm conditions to commence certain signature analysis or to activate cameras or other sensors on the network. Thus, an event in a particular sensor cluster: be it noise or a vehicle or motion, can activate a microphone or camera, multiple cameras and/or other sensors in the vicinity. This sensor action will provide unique sensor information fused with imaging for precise viewing of the threat incident.

In addition to the added sensor modalities, Avaak plans to improve the optical capabilities of its camera nodes with advanced imagers (2MPixels) and lenses (possibly including small zoom lenses). Zooming capabilities for micro-cameras will become possible via micro-fluidic (MEM) devices requiring very little power and surface area (new technology).

Audio capabilities will be provided by a 4mmX4mm CMOS MEMS microphone with power-down mode features that reduce current consumption when the microphone not in use.

The proposed multi-modal sensor platform will be based on the AV-18 communications and processing module shown below (Figure 4).

[redacted]

Figure 4 Avaak AV-18 communications, processing (left) and imaging modules (right)

1.3.3.1 Task 3.1 Motion PIR Sensor Modality

The Passive Infra Red (PIR) motion sensor will use infrared to monitor the movement of "warm" bodies in a specific area and will "alarm" either to start other actions on the same sensor node or other areas of the system (depending on programmed rules) if motion is detected. The PIR sensor is able to detect humans and provide an estimation of the direction of movement. The possibility to perform object tracking using multiple sensors provides a good foundation for the sensor fusion function in this application.

Objects that generate heat also generate infrared radiation. The wavelength of infrared radiation is longer than the wavelength of visible light. It can not be seen, but it can be detected by a pyroelectric sensor. This sensor is made of a crystalline material that generates an electric charge when exposed to infrared radiation (i.e. heat). The amount of charge is proportional to the amount of radiation. Pyroelectric elements are sensitive to radiation over a wide range, therefore a filter window is placed before the sensor to limit incoming radiation to 8-10 *um* range, which includes the infrared radiation from human bodies.

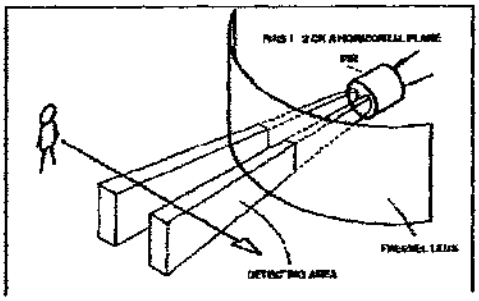

Figure 5 Motion detection with a PIR sensor

The motion sensor's range of detection will approximately 40-50 feet. A picture of a wireless, battery operated PIR motion sensor that Avaak is developing for use by Naval Expeditionary Forces (under a contract with SPAWAR) is shown in Figure 6. This sensor node utilizes a CR2 lithium-ion battery that enables it to have years of field life. It is enclosed in a 2inx2in plastic enclosure and weighs less than 2 ounces.

Development of the Motion sensor modality will consist of the following tasks:

- Motion Sensor Specification
- Component Selection
- Hardware Low Level Design
- Firmware Design
- Firmware Implementation
- DVT
- Integration

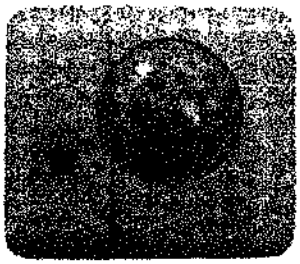

Figure 6 Avaak PIR Motion Sensor

1.3.3.2 Task 3.2 Acoustic Sensor Modality

The acoustic sensor incorporated in this platform will use a Micro- Electro-Mechanical System (MEMS) microphone with full audible spectral coverage, which we suggest be limited to 2KHz (i.e. 100-2000Hz). The MEMS sensor we propose using requires only 100uA of current, has excellent sensitivity and is omni-directional. The microphone is 5mm in diameter and will be connected to an analog conditioning circuitry and then an A/D for further processing. The analog circuitry that amplifies and filters the sensor output requires less than 100uA.

The sampling rate shall be ~ 5KHz. The sensor signal will be stored and then connected to a processor for future signal analysis, signature detection and identification or for streaming to the wireless link. The acoustic modality will be able to perform some crude detection of analog signals (e.g. signal acquisitions that occur after a certain analog threshold). The aim is to have a sensor with excellent sensitivity and signal processing capabilities at very low power requirements. The signal bandwidth of this system will be determined further down the line during the design cycle with help from ONR and expeditionary forces. Avaak suggests using 2KHz bandwidth but this parameter can be changed.

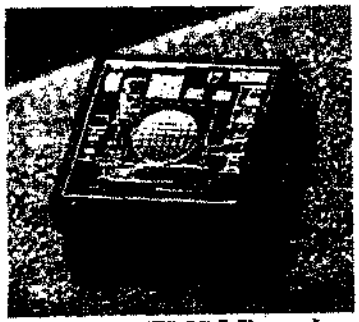

Figure 7 MEMS Microphone, 5x5mm with 1V output at -40dB @1KHz

The tasks associated with the development of the acoustic (microphone) sensor are as follows:

- Acoustic Sensor Specification

- Component Selection
- Hardware Low Level Design
- Firmware Design
- Algorithm Design
- Mechanical Design
- General Firmware Implementation
- DVT

1.3.4 Task 4 - WSN WiFi Network Gateway/Hub (Vision Network Gateway)

The network gateway/hub that Avaak is proposing will combine the capabilities of the currently available Avaak AV-20 (Figure 7) high performance base-station/hub that provides management and aggregation of sensor network data with the ability to bridge the WSN to a WiFi IP network. The Avaak Vision Network Gateway (Figure 8) will coordinate routing, aggregate data packets, collects statistics, and interface with the host computing device to control the sensor network. The network gateway/hub will provide a well defined application interface which allows programmatic control of the sensor network from loosely coupled remote console application as described below.

The network gateway/hub will be a self contained multi-protocol device. It will be AC powered and/or battery powered.

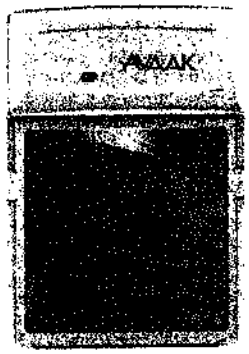

Figure 8 Avaak AV-20 Mobile Base-station for Wireless Sensor Networks

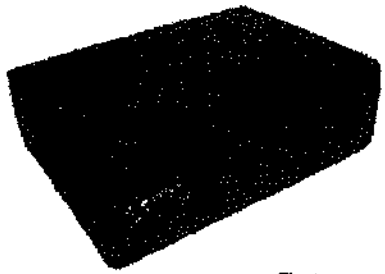

Figure 9 Avaak Vision Network High-Performance Gateway for Wireless Sensor Networks

It is expected that the technical specifications of the Avaak Vision Network gateway will be similar to the AV-20 specs shown below:

Specifications	AV-20
Communication protocol	Packet switching, frequency hop
Frequency operating range	2400-2500MHz
Modulation type	GFSK. BT = 0.6
Frequency step	1MHz
Frequency accuracy	+/-30ppm
Frequency switching speed	<200usec
Data rate (Inbound)	Programmable: 250Kb/s, 1Mb/s, 2Mb/s
Power	5 VDC @50mA
Operating temperature	0 to +70C ambient
RF power output	-10 to +10dBm with 5dB Step
Sensitivity	-100dBm @ 250Kb/s
Antenna	2 antenna Diversity
Antenna Gain	1.6dBi
Networking	Star/Mesh Configuration

The following tasks pertain to the development of the WSN Vision Network Gateway/Bridge:

- Update AV-20 Specification to account for changes required by this program
- Update PCB Card – modify PCB design to incorporate necessary changes specific for this program
- PCB Layout – layout the PCB card
- PCB Fabrication – fabricate the PCB assembly and insert all the electronic components
- Mechanical Design – Design mechanical packaging for the gateway
- Firmware Modifications – modify and incorporate additional features into the software specific to this program
- Mechanical Packaging – Build mechanical package prototype
- Integration/Test – integrate hardware, software, networking with mechanical package
- Platform 1st Pass Proto test

1.3.4.1 Task 4.1 Laboratory Demonstration of System Components

Avaak proposes to demonstrate a fully integrated multi-modal sensor prototype platform along with some rudimentary processing and network capabilities at the end of the base year of this proposal. This demonstration will be a laboratory demonstration at Avaak's facilities.

1.4 FY09 Tasks

1.4.1 Task 5 Image Object Classification Implementation

This task consists of the implementation of algorithms that achieve simple/crude object recognition/characterization on-board the multi-modal node to identify objects such as people, airplanes or cars. The locally run algorithms will "watch" their internal video streams and extract descriptions of all relevant objects. Each multi-modal node will employ sophisticated and power-efficient methods to detect all relevant objects in the camera's view. Algorithms for classification of objects into specific types as illustrated in Figure 9 will also be incorporated.

These basic functions of image characterization at the node level are nothing by themselves. They need to be part of a truly effective security system. To achieve this, the system needs to be

- Scalable. To effectively monitor a large area, the system has to scale to hundreds, perhaps thousands, of sensors. It needs to be able to integrate and fuse information over both space and time

- Integrated. Avaak realizes that video surveillance is a key part of a total solution, but not a solution unto itself. Any system such as the one described must be able to integrate seamlessly into other physical security systems such as high resolution PTZ cameras to provide actionable real alerts that increase their effectiveness.

- Operationally effective. The classification algorithms must be well tuned to provide high system reliability, low false alarm rates and ease of use.

Figure 10 Crude Object Detection and Classification

The following will be accomplished during this task:

- Develop Imaging "Footprint" Algorithms (based on Eigen-analysis)

- Algorithm Design & simulations
- Power Consumption Vs. Algorithm Tradeoff Analysis
- Data Model and Data Analysis
- MatLab Simulations
- Firmware Implementation
- Simulant Testing

1.4.2 Task 6 - Development of Localization via GPS

The integration of GPS on small platforms is still problematic due to hardware, antenna and battery limitations; though this difficulty is currently mitigated by the appearance of integrated GPS solutions on a single chip. These solutions, just being introduced to the market, require external memory, which will be a small part of the overall memory we plan to place in the multi-modal node.

The need for every multi-modal node to have GPS capabilities will have to be assessed during this phase. We will also assess how often GPS coordinates are obtained from the satellite since this an expensive power operation for battery powered devices. Avaak proposes to incorporate an accelerometer on GPS nodes such that these "know" when they have been moved and can automatically re-acquire coordinates. Otherwise GPS acquisition would only occur when first deployed and otherwise very infrequently.

This task involves:

- HW design (GPS chip + memory)
- Adapting the node antenna to cover both WSN and GPS bands
- Utilization and Power evaluation (GPS needs be applied quite infrequently)
- System test for GPS sensitivity and accuracy

1.4.3 Task 7 RF Range Enhancements/Antenna Systems

Radio communications range is a major consideration for agile sensor networks. Most networks utilize a low power radio that integrates the radio functions and the modem to produce an integrated solution. Because of the limitations in ASIC power delivery (as geometries shrink) these radios deliver approximately 0dBm (1mW) maximum output power and approximately –85dBm sensitivity for data rates of 2Mb/s. Avaak's choice is to supplement these ASICs with proprietary technologies that enhance performance on both sides by approximately 20dB. Two-way TX/RX dynamic range, in comparison to existing networks, is therefore in the order of 40dB, which is a significant enhancement. Avaak's sensor nodes have the best range of any sensor node in the market today and that is achieved with very little extra power required from the battery. (In addition, power requirements of integrated radios keep dropping with new radio architectures, which help conserve power.) In addition to radio performance, the antenna is probably the most critical part of the radio system for achieving desired transmission ranges. Avaak believes that the commercial WSN market has neglected this critical parameter, perhaps because most of the companies involved possess only software and networking backgrounds. Avaak has vast radio experience and has incorporated a focus on antenna performance in its

[redacted]

video sensor nodes. Miniature antennas are a rather new discipline in the market, and one that will receive more attention in the future as the adoption of WSN ramps up.

The use of ceramic materials enables the size of the antenna to shrink but the design of an omni-directional antenna with a good gain (donut radiation pattern) will be a major challenge in this proposed network's design.

Our plan is to enlarge our sensor node size (from 1 cu inch to ~4-5 cu inches) to allow for a larger battery (to increase transmitted power and lifetime in the field) and an enhanced antenna (for enhanced communications capabilities). An antenna with some directionality will be necessary on the hub (base station) to achieve the wireless range required by the network. Avaak estimates that a 2Km range, with a sensor node placed close to the ground, might require a link with up to ~140dB path-loss using an omni-directional hub antenna, but only ~120dB with a directional antenna (Avaak's current camera node system has been shown in field tests to have a ~1Km range with a 20dBi hub antenna).

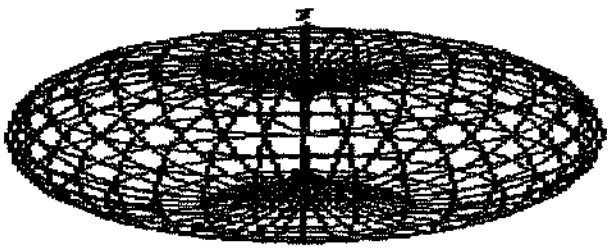

Figure 11 Omni-directional antenna pattern with gain

The following tasks will be performed:

- Antenna Design Sensor Node
- Antenna Design Hub
- Antenna Implementation Node
- Antenna Implementation Hub
- Antenna System test free-space (chamber)
- Antenna System field test

1.4.4 Task 8 Network Software Application Development

The ability to view and control the multi-modal sensor network in real-time from anywhere in the combat theater and to provide situational awareness to the war-fighters, regardless of their location, is imperative. Sensor systems must be able to provide user interfaces that can be mobile or static and that make use of network-centric approaches and multi-tier software architectures similar to what makes the Internet such a powerful tool today. Visualization tools that display sensor statistics as well as battery power and other reporting and diagnostic tools will be created.

Avaak proposes to develop a multi-tier approach to network control by bridging the Vision Network to an IP network that can provide any user, connected to the Net (with the appropriate credentials) to view and control a deployed WSN. The network bridge will be achieved via a small stand-alone gateway hub that speaks both the WSN protocol and IP. Direct IP streams for certain data types as well as SOAP and XML will be used to command the camera nodes, retrieve information, tag image data and display what is happening on the network in real-time. A multi-tiered approach will also be used to create a presentation layer, a data layer and a physical layer that can work on many different user interface devices.

Avaak proposes to implement the user interface application architecture based on a .NET framework. For the most part, all connections between the services will use XML or socket protocols to create a robust connection; however other standards will be used to interact with video and audio data that may require faster processing through the network.

The following tasks will comprise the development of the WSN service oriented software application and GUI:

- UI Implementation – implementation of the user interfaces
- Object Framework – implementation of the object framework
- XML DDFs – implementation of the interfaces and data definition
- Main Objects and Interfaces – Implementation of the object brokers

1.4.4.1 Task 8.1 GUI

A web-based GUI will be developed to support the large tactical WSN grid. The primary purpose of the GUI will be for sensor status and reporting. Figure 11 shows a sample GUI created for Expeditionary Forces on a previous project.

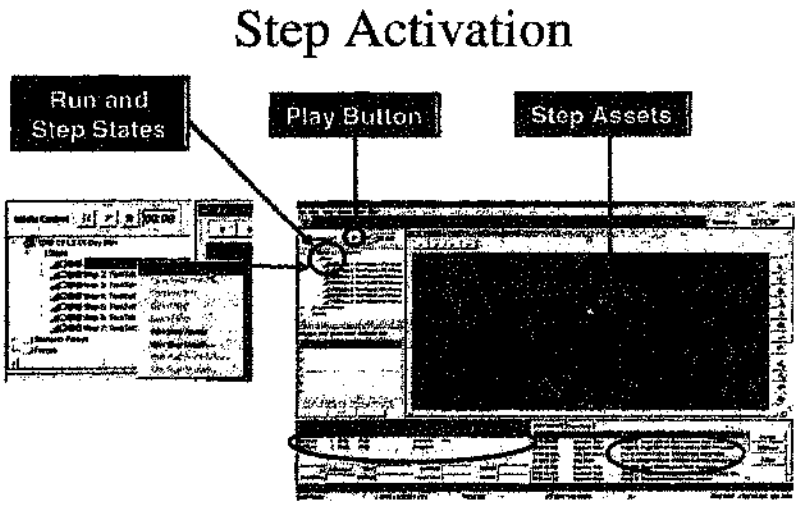

Figure 12 Sample GUI

1.4.4.2 Task 8.2 Sensor Interface

The GUI will provide the ability to display the three sensor modalities being contemplated initially for this system and integrate additional sensor types at a later date

The following tasks will comprise the development of the WSN service oriented software (object brokers), GUI and reporting functions:

- GUI Layout
- Rule Engine Implementation
- High Resolution PTZ camera cueing
- Network configuration
- System Status and alarms
- Interfaces to other systems?
- Unit Test
- Software integration
- Software Test

A screen display will show several network parameters and QOS status elements, based on the indicators are readily available from the network and are suited for visual presentation.

1.4.4.3 Task 8.3 Sensor Data Reporting

Data responses from a requested sensor will be displayed in a format specific to the type of sensor. Retrieved video will be displayed with a player equipped with industry standard controls.

1.4.4.4 Task 8.4 Simple Rule Engine

In addition to the simple alerts and alarms the system will enable the cueing of other network systems such as high resolution PTZ cameras on the network.

1.4.4.5 Task 8.5 Data Processing

It is almost a certainty that these large tactical networks will *not* want to permanently store all of the millions of bits of sensory second-by-second data coming from thousands of nodes. Critical to the success of this *smart* WSN is its ability to understand, manage and optimize the data flow in the network and make highly pre-processed data available at any level within the command and control chain. The ability to query by proxy or live within the network gives accurate in-network information that enables additional network optimizations. Questions of what data is needed, where, when and how best to process can then be addressed later.

1.4.5 Task 9 - Build and Test all Sensor Modalities for Large Scale Deployment

[redacted]

This task consists of building 100 sensor nodes of the various modalities described in this proposal (acoustic, motion, imaging and GPS) and implementing the cross-cueing and sensor fusion functionalities that can only be performed once the capabilities of each sensor and the network is understood.

Sensors will be manufactured using COTS products and will utilize the currently available Avaak AV-18V imaging sensor node and Avaak Vision Network Gateway as the base line. Integration of the sensor network with the gateways and service oriented architecture application software will be performed during this task. Each sensor will be tested against it's agreed upon specification both as a unit and in the system.

This task will also include the writing and implementation of a test plan both at the node level and at the system level.

- Multi-modal Sensor Network Construction
  - Multi-modal sensor operation
  - Testing image processing implementation
  - Testing implementation of PTZ cueing functionality at the network level
- Fabrication of the various multi-modal senso to support a test of 100 sensor in the field
- Platform Test Plan
- System Test Plan
- Integration of all the sensors in the network with the rest of the system
- System test of multi-sensor
- Demonstration of sensor modalities – to include 100 sensors nodes (some with GPS capabilities) and Gateways placed over a large area
- Demonstration of system capabilities including software architecture and graphical user interface

1.5 FY08 Development

From an Operational Utility perspective this phase demonstrates the goal to achieve interoperability of multiple sensor modalities on a single node in a wireless network. This effort will also demonstrate the ability to perform JPEG image processing on the imaging node, and demonstrate thresholding on the motion and acoustic components of the node.

The following are the most significant milestones of the technology development process for the FY08 program year:

- System Specifications
  - March 2008 - All Specs Ready
- Motion Sensor Modality
  - May 2008 – 1st Article motion modality
- Acoustic Sensor Modality
  - July 2008 - 1st Article acoustic modality

- Modified Video Sensor Platform (AV-18-V)
  - August 2008 - 1st Article modified video sensor
- WSN WiFi Bridge (Gateway)
  - September 2008 - 1st Article Gateway/Bridge hub
- January 2008 - Demonstration of prototype multi-modal sensor nodes

1.5.1 Outputs of FY08 Effort

- System Design Specification
- Sensor Prototypes
- Working models of multi-modal sensor to include video, acoustic and motion sensors in a single cost effective, light weight platform
- Progress Reports (Quarterly)

1.6 FY09 Development (Option 1)

From an Operational Utility perspective, this effort demonstrates the goal to achieve automatic object analysis and cueing of high resolution PTZ cameras on the network. This effort will also demonstrate the ability to automate tactical goals with limited or no supervision. At the end of this effort a 100 node system will be demonstrated. The system's capabilities will allow for network functionality over a 2 sq Km area.

Avaak's effort in this phase will provide automated techniques to aggregate sensor data and other data from other sources. It will also provide a rules based engine for each sensor modality. The rule engine will also define triggers and exclusions and determine positive events.

HUMINT capabilities will also be demonstrated such as imaging fused with audio and motion information from a single imaging node.

This effort will also demonstrate the ability to:

- Automate execution of tactical goals with limited or no supervision
- Minimize bandwidth use by forwarding processed information and knowledge
- Create sensors with situational awareness/localization – GPS localization by the network is essential to be able to correlate events with acquired sensor data.

The following are the most significant milestones of the technology development process for the FY09 program year:

- Video Object Classifications Algorithms
  - September 2009 – Algorithm demonstration
- GPS Integration
  - July 2009 – Inclusion of GPS capabilities on multi-modal node
- Antenna Systems Node/Gateways
  - May 2009 – Design of both antenna systems complete
- Network Control Software

[redacted]

- September – 1st pass of User API complete
- Sensor Packaging
  - September – 1st pass packaging
- Multi-modal Agile Sensor Network for GWOT complete
  - February 2010 - Demonstration of multiple modalities of sensors and SOA software

1.6.1 Outputs of FY09 Effort

- 100 working models of multi-modal sensor nodes
- TBD working models of multi-modal sensor nodes that include GPS capabilities
- 10 Working models of network gateways/bridges
- Final Report

Software will be delivered as executable code.

[redacted]

5.B. Detailed Statement of Work

5.B.1 Base Program

The Base Program is organized into two overlapping phases; Phase 1 is 14 months in duration and Phase 2 is 24 months. Phase 1 will culminate in the laboratory demonstration of a monochrome VGA sensor (480 x 640 pixels) integrated with an off-chip FPGA (field programmable gate array) image accumulator. Phase 2 will conclude with the field demonstration of a portable wireless camera with a color ~ 20 MegaPixel image sensor monolithically integrated with an image accumulator/compression engine and frame buffer.

A proposed Option would lead to the development and laboratory demonstration of a 34 MP imager employing a multi-chip module design. If accepted, the Option effort would commence at the earliest in the middle of Year 2 and run for 18 months in parallel with the primary effort. (The Option could be started at any time after Year2-Q3.) The Option program will employ the main design elements developed in the early part of the Phase 2 effort. The Option effort will require additional interface circuit design, fabrication of two different IC's (the image sensor array and a custom memory chip) and their integration into a multi-chip module.

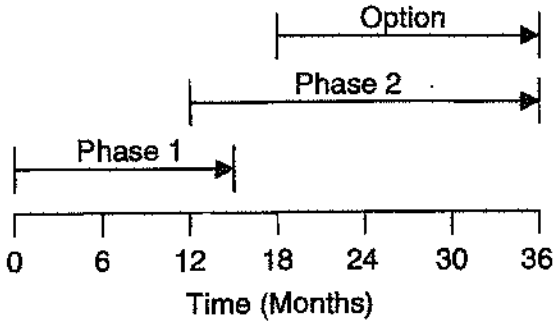

Figure 5.B-1 – Time line for the two-phase program plus proposed option.

The steps and required fabrication runs are summarized below. We show this for both the Base and the Option programs. The Option Program builds upon intermediate results of the Base Program and would commence at the start of Year 3.

Program Summary and Fabrication Schedule: Base and Option programs

Base Program: 20 MP single chip image sensor and camera
Duration: 36 Months
Steps and planned fabrication runs:

1. Test structures & VGA array for off-chip image accumulator – 1 fabrication run
   Fab 1: 14 mm^2 in IBM7RF: ($45k) **Y1-Q1**
2. 1.2 MP sensor (2x2 VGA) plus 1xVGA 1TSRAM – 2 fabrication runs
   Fab 2: 25 mm^2 in IBM7RF: ($70k) **Y1-Q3**
   Fab 3: 25 mm^2 in IBM7RF: ($70k) **Y2-Q1** (if required)
3. 20 MP (8 x 8 VGA) plus 2x2 VGA 1TSRAM – 2 fabrication runs
   Fab 4: IBM CIMG7 Full Run ($280k) **Y2-Q4**

Fab 5: IBM CIMG7 Full Run ($280k) **Y3-Q2** (if required)

4. Camera (wireless) integration and test

Option Program: 34 MP imager (2 Chip Multi-chip module)
Duration: 18 months
Steps and planned fabrication runs:

1. VGA size prototype: Sensor plus separate memory IC (~ 4 Mbit)
   Fab O1: 2 chips each 10 mm^2 in IBM7RF: ($72k) **Y2-Q4**
2. 34 MP sensor IC & memory IC
   Fab O2: IBM CIMG7 Full Run ($280k) **Y3-Q2**
   Fab O3: IBM CIMG7 Full Run ($280k) **Y3-Q2** (backup if needed)
3. MCM Integration and Lab Demonstration
4. Camera integration and test

Table 5.B -1 below summarizes both the program milestones (all items in the table) and the program deliverables *(italicized text)*, broken out by function and program phase. We discuss each of the table's items in the following text.

	Task	Base Program Phase 1	Base Program Phase 2
1	**Pixel Development**	(Fab 1: test structures) *Test Report and Pixel Design Choice*	n.a.
2	**Image Sensor**	(Fab 1: VGA Sensor) *2x2 VGA Imager CDR*	*20MP Image Sensor CDR* 20MP Sensor Layout
3	**Image Accumulator**	(FPGA Image Accumulator) *(1x VGA image accumulator design review)*	*Image Accumulator CDR* Image Accumulator Layout
4	**Imager ASIC**	(Fab 2: 2x2 VGA with 1x VGA frame buffer) (Fab 3: 2x2 VGA with 1x VGA frame buffer) if needed	*20MP ASIC CDR* Fab 4: 20MP Imager Fab 5: 20MP Imager (if req.)
5	**Electronics**	2x2 VGA Sensor Controller	*20MP Camera Elecs. CDR* 20MP Field Camera Elecs.
6	**Optics**	VGA Camera Optics	20MP Camera Optics
7	**Package/Integration**	*Lab Cam CDR* Laboratory Camera	*System/Package CDR* 20MP Field Camera
8	**Wireless Camera Integration**	n.a.	*Wireless Camera CDR* Wireless 20MP Camera
9	**Test**	*Lab Demo and Report*	*Field Demo and Report*

Table 5.B-1 – Milestones (all) and deliverables (*italicized*), organized by task and program phase.

Base Program Phase 1

[redacted]

The first goal of the Phase 1 Base Program is to design, fabricate and characterize a VGA size monochrome DPC Image Sensor. The sensor image accumulator and compression engine will be implemented by an off-chip FPGA, the design of which will be used as the basis for the ASIC-based image processing engine to be developed in the next program phase. Architectural studies and analysis for the image accumulator that will be built in Phase 2 will be started in Phase 1 and by the conclusion of Phase 1 a 2x2 VGA imager with 1x VGA frame buffer will be designed and submitted for fabrication.

Task 1-1: Image Sensor
Approach/Methodology: The first step in the image sensor development task will be the fabrication of several test circuits employing the MOSIS multi-user fabrication service to assess different pixel design options. This will enable us to employ an IBM 0.18 μm fabrication technology at a more reasonable cost than a dedicated run. Our existing DPC designs range from 3 to 5 transistors per pixel and differ in the details of the design of the feedback digital to analog converter (DAC) at each pixel. The noise of the DAC is a critical factor in the overall sensor performance and this step will enable us to choose the best design.
Challenges/Problems: Moderate risk. Pixel noise is determined by fundamental properties of the circuits such as switch capacitor reset noise and by fabrication related imperfections such as photodiode leakage current. Current estimates based on calculations and fabrication foundry provided data indicate that the design goal of 0.1 lux low light response with 15 dB SNR is achievable but this must be verified through test structure fabrication and laboratory measurements before committing to a specific pixel design.
Mitigation Plans: If current DAC designs are found to have excessive noise that would compromise the program goals we can employ alternative DAC designs; ones that employ either the so-called tapered reset that has already been employed in other imager designs or an active reset technique developed by us. These alternatives would require more transistors per pixel, which will increase the overall pixel size and the power consumption. If we are forced to adopt this mitigation plan new system performance specifications will be detailed. However, even if the mitigation plan is adopted we do not anticipate a degradation of the performance specifications given above by more than a factor of 2. The goal in this aspect of the work plan is to meet the program performance goals with a minimum number of transistors per pixel and minimum power consumption.
Deliverables: *Test report and pixel design choice*

Task 1-2: Image Sensor
Approach/Methodology: In the first run we will build a VGA pixel array employing our current 5T design. This will be used to develop the FPGA based image accumulator. The test results of alternative pixel designs created in Task 1-1 will guide the design of the next level design, a 2x2 VGA array with integrated image accumulation engine.
Challenges/Problems: Low risk.
Mitigation Plans: We have a working design already that can serve as our base design if preferable alternatives are not identified.
Deliverables: 2x2 *VGA Image Sensor CDR*

Task 1-3: Image Accumulator
Approach/Methodology: A FPGA (field programmable gate array) based Image Accumulator will be designed and built. Another function of the Image Accumulator will be the dynamic control of the DAC gain for auto-ranging and extension of the sensor dynamic range. This task will enable laboratory demonstration of a VGA Image Sensor. This step also will provide algorithm verification and VHDL level design elements for the design of the on-chip image accumulator. This stage may be developed prior to completion of the image sensor chip by employing simulated image sensor output data.
Challenges/Problems: Low risk.
Mitigation Plans: A similar project is under way in the PI's University-based research laboratory; the requirements of this task are similar.
Deliverables: *1x VGA image accumulator design review*

Task 1-4: Imager ASIC
Approach/Methodology: We will integrate the best current design of the 2x2 VGA sensor with 1x VGA image accumulator and frame buffer and submit the design for fabrication through MOSIS; this is the Fab2 run.
Challenges/Problems: With any IC design there is a chance of design and layout errors or unanticipated factors that limit performance.
Mitigation Plans: Extensive simulations employing Cadence design tools will be conducted. A second fabrication run (Fab3) is also factored into the program.
Deliverables: none

Task 1-5: Electronics
Approach/Methodology: The off-chip supporting electronics will be developed for the 2x2 VGA sensor. We will employ a low power FPGA for this purpose. The other required power supply circuits will be designed and a controller circuit board that integrates the FPGA and these circuits will be built with COTS discrete components.
Challenges/Problems: low risk
Mitigation Plans: Similar control electronics have been designed in the PI's University lab.
Deliverables: none

Task 1-6: Optics
Approach/Methodology: Commercial-off-the-shelf optics will be employed in the laboratory camera. The choice of optics will be determined by the final pixel size determined in Task 1-1 and the operational requirements of the camera such as the field of view, magnification, depth of field, and flatness of field.
Challenges/Problems: low risk
Mitigation Plans: none required
Deliverables: none

Task 1-7: Package Integration
Approach/Methodology: Size, weight, and power consumption are not critically important in this phase of the project but we will minimize all three to create a laboratory camera that is relatively portable and capable of off-site imaging demonstrations.

[redacted]

Challenges/Problems: low risk
Mitigation Plans: none required
Deliverables: *Lab Camera CDR*

Task 1-9: Test
Approach/Methodology: Laboratory measurements and characterization of the image sensor dynamic range, noise and low light response, quantum efficiency, and linearity will be performed. The image sensor DAC gain, adjustable dynamic range feature will be demonstrated and characterized. The image accumulation circuit will be demonstrated by capturing images in both raw format and as a wavelet transform.
Challenges/Problems: Quantitative image sensor characterization is experimentally challenging and considerable laboratory facilities are required to carry out such measurements.
Mitigation Plans: University of Rochester testing facilities will be employed in this task.
Deliverables: *Lab Imaging Demonstration and Test Report*

Base Program Phase 2

The goal of the second program phase is to design, fabricate and characterize a a 20 MegaPixel Imager ASIC composed of the 8x8 VGA Image Sensor and the Image Accumulation Subsytem. The sensor will incorporate dynamic range scaling through automated control of the DAC gain and it will be reconfigurable to operate in low power sentry mode. The Imaging ASIC will be built into a compact surveillance camera with a standard data interface that will be integrated with a selected wireless platform in collaboration with RLW, Inc.

Task 2-2: Image Sensor
Approach/Methodology: The 20MP image sensor will be based on the design demonstrated in the 2x2 VGA sensor developed in Phase 1. Other than scaling the pixel count and resizing various drive transistors to accommodate the longer signal traces the only other new aspects of the design will be the addition of the color filter array and microlens array to optimize light collection efficiency. These are both standard features available in the IBM CIMG process but optimization is required for the DPC pixel size and structure.
Challenges/Problems: Adapting standard IBM process steps to the custom pixel configuration of the DPC imager
Mitigation Plans: Close collaboration with foundry will be important in this task.
Deliverables: *20 MP Sensor CDR*

Task 2-3: Image Accumulator
Approach/Methodology: The preferred approach is to integrate the entire image accumulator including the computational core and the frame buffer memory into a monolithic silicon design. Ultimately this will lead to the most compact and lowest power design. The computational structures developed in the Phase effort will scaled up in size and transferred to this design. The adaptive DAC gain/dynamic range feature also will be implemented in the Phase 2 Image Accumulator.

[redacted]

Challenges/Problems: The greatest challenge is the frame buffer physical size. As discussed above the memory per pixel requires 2.5 x the area of the pixel itself. We must work to identify the most efficient memory design and other techniques such as employing a reduced size frame buffer as described above.
Mitigation Plans: We will employ a 1T SRAM rather than the standard 6T SRAM design if possible. We also will employ a frame buffer that is only a fraction of the size of the entire imaging array and compensate by the means described above in Section 5.A.4.
Deliverables: *Image Accumulator CDR*

Task 2-4: Imaging ASIC
Approach/Methodology: The image sensor and the image accumulator structures will be integrated into the imaging ASIC. The simulation, layout and verification of the design will be conducted employing Cadence IC design tools. The final design will be fabricated to the foundry, Fab4.
Challenges/Problems: Complexity of combined design and potential for design layout errors.
Mitigation Plans: An extensive simulation and verification process will be conducted. A second fabrication run is planned (Fab5) to both refine the initial design and to serve as a contingency option.
Deliverables: *Final CDR of the 20 MP Imager ASIC prior to fabrication submission.*

Task 2-5: Electronics
Approach/Methodology: The supporting electronics design must address several issues including provision of low noise power supplies to the Imaging ASIC, providing the set of clock and control signals to the ASIC and providing the data interface to download image data from the ASIC frame buffer. The first two sets of considerations will be addressed in Task 1-4 and those solutions will translate to the Phase 2 project. We will employ a standard interface for transferring the data from the imager ASIC frame buffer, for example USB 2.0 (480 Mbit/sec) will be capable of handling the transfer of compressed images at our anticipated data rates. The electronics package also will provide the interface to enable the user to configure the imaging ASIC to operate in the sentry mode or in various full operation mode.
Challenges/Problems: Minimization of power
Mitigation Plans: Include as much of the control function as possible on chip. Employ a low power FPGA for the remainder of off chip functionality.
Deliverables: *20 MP Camera Electronics CDR package*

Task 2-6: Optics
Approach/Methodology: The performance specifications of the camera optics will be determined by the specific applications and transition opportunities identified as the program proceeds. Such requirements will arise through continued discussions with ONR program officers and unless a specific custom requirement is identified we will employ a "middle of the road" design. Commercial off the shelf optics will be employed to the greatest possible extent. However, to remain within the size and weight constraints

(2 cubic inch and 50 grams) it may be necessary to design a custom lens package employing commercially available light-weight plastic lenses.
Challenges/Problems: Staying within the size and weight constraint while providing the required imaging performance.
Mitigation Plans: There is an extremely deep base of optical design and fabrication expertise in Rochester, NY that may be leveraged to help create the required design.
Deliverables: *none*

Task 2-7: Package Integration
Approach/Methodology: The overall 20MP camera design including electronic, optical and mechanical features is addressed in this task.
Challenges/Problems: The central concern is to remain within the size and weight constraint and to minimize the complexity of prototype manufacturing.
Mitigation Plans: A large number of camera optical and mechanical packages are available commercially. We will employ such commercially available options to the greatest extent allowed by the program needs.
Deliverables: *System/Package CDR*

Task 2-8: Wireless Camera Integration
Approach/Methodology: The primary consideration in this task is to provide a wireless link that is capable of transmitting the large amounts of data than can be generated by the imager in full operation (non-sentry) mode. Several factors come into play such as the operating mode and frame rate, compression ratio and compression scheme i.e., MPEG vs. motion JPEG. Existing wireless radios such as Bluetooth and Zigbee are far below this required data rate for real time remote viewing. Current ultra-wide-band and 802.11 N radios will be assessed at this stage in the program and the most power efficient solution will be selected.
Challenges/Problems: Meeting the data rate requirements within a standard wireless data transmission protocol.
Mitigation Plans: Possibly employ parallel data transfer paths.
Deliverables: *Wireless Camera CDR*

Task 2-9: Test
Approach/Methodology: The 20MP camera produced in the second phase of the program will be tested both in the laboratory to quantitatively assess its performance and in real field situations to obtain a more qualitative user assessment of the camera performance and utility.
Challenges/Problems:
Mitigation Plans:
Deliverables: *Final Test Report*

5.B.2 Option Program

We also propose a program Option in which a 34 MegaPixel imager employing a multi-chip module design will be developed. This may commence at any time from Year

[redacted]

2, Quarter 3 onward. Since the Option will build upon work accomplished in the Base Program this is the earliest that the Option can be started.

Table 5.B-2 below summarizes both the Option program milestones (all items in the table) and the program deliverables *(italicized text)*, broken out by function and program phase. We discuss each of the table's items in the following text.

	Task	Option Program
1	**Pixel Development**	n.a
2	**Image Sensor**	(Fab O1: VGA Sensor for Off-Chip Frame Buffer)
3	**Memory IC**	Decision on custom memory IC vs. commercial (Fab O1: Frame Buffer IC if needed)
4	**Imager MCM**	*MCM CDR* (Fab O2: 34 MP image sensor IC and memory IC if needed) (Fab O3: repeat fabrication if needed)
5	**Electronics**	MCM Imager Controller Electronics
6	**Optics**	Camera optics selection
7	**Package/Integration**	*Lab Cam CDR* Laboratory Camera
8	**Wireless Camera Integration**	n.a.
9	**Test**	*Lab Demo and Report*

Task O-2: Image Sensor
Approach/Methodology: The design of the image sensor chip and image accumulation computational block will be the same as the base program image sensor arrays. The chief difference will be the addition of data multiplexing and memory interface circuits to enable transmission of the image data to the off-chip memory.
Challenges/Problems: None beyond those in the base program.
Mitigation Plans:
Deliverables:

Task O-3: Memory IC
Approach/Methodology: We will conduct a detailed study of the feasibility of employing commercial memory chips for the frame buffer. As expressed earlier the concern is the data bottleneck due to the limited data pipe width of standard memory chips. It is highly preferable to be able to employ commercial memory, however if this proves impractical a custom memory IC will be designed and fabricated.
Challenges/Problems: Complexity of designing a custom frame buffer IC.
Mitigation Plans: Employ third party memory intellectual property blocks. This is a highly developed area with several vendors (Mosys, Novelics, Virage Logic) offering memory IP for embedded applications.
Deliverables:

Task O-4: Imager MCM
Approach/Methodology: We anticipate employing a ceramic substrate MCM with wire bond inter-chip connections. A design study will determine the optimal architectural approach i.e., how many memory chips, the number of data paths, etc..
Challenges/Problems: Power minimization.
Mitigation Plans:
Deliverables: *MCM CDR*

Task O-5: Electronics
Approach/Methodology: The external MCM control electronics will be similar to that developed for the 20 MP imager. However, the multi-chip design adds a bit of complexity to the base program design.
Challenges/Problems: Minimization of power as in the Base program.
Mitigation Plans: Include as much of the control function as possible on chip. Employ a low power FPGA for the remainder of off chip functionality.
Deliverables:

Task O-6: Optics
Approach/Methodology: We will employ commercially available optics. The 34 MP imaging array we propose to build is slightly smaller than commercial 2/3 frame digital SLR camera image sensors, which are 16 x 24 mm. Therefore we will have a wide array of lens choices.
Challenges/Problems: low risk
Mitigation Plans:
Deliverables:

Task O-7: Package Integration
Approach/Methodology: This refers to integration of the imaging MCM into a camera package. Given the large image sensor area optical alignment is especially critical to obtain an in-focus image across the imaging array.
Challenges/Problems: Minimizing weight while maintaining mechanical stability.
Mitigation Plans: We will explore adapting a commercial digital SLR camera body for the laboratory demonstration.
Deliverables: *Lab Camera CDR*

Task O-9: Test
Approach/Methodology: Similar to the Base Program.
Challenges/Problems:
Mitigation Plans:
Deliverables: *Final Report*

[redacted]